Intense Pulsed Light-Driven Flip-Chip Bonding for Energy-Efficient and Sustainable Packaging

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Advanced Semiconductor Packaging

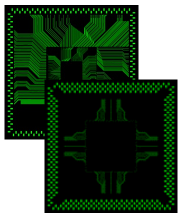
Contents

❖ Research Introduction - Prof. Hak-Sung Kim

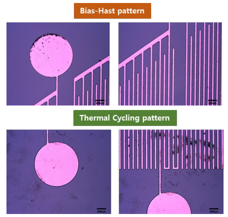
- Principal Investigator: Prof. Hak-Sung Kim
- Major Academic & Career Background
  - ✓ Professor, Hanyang University [2010 ~ Present]
  - ✓ Research Distinguished Professor, Hanyang University [2020 ~ Present]
  - ✓ Director, Advanced Semiconductor Packaging Research Center, Hanyang University [2022 ~ Present]
  - ✓ Vice-President, Korea Microelectronics and Packaging Society [2024 ~ Present]

- Research Experience: 30+ students under Prof. Kim's supervision
- Patents: 170+ domestic and international publications
- Research Performance: 198+ projects
- SCI Publications: 222+ international / 29+ domestic
  - ✓ ACS Applied Materials & Interfaces, in press (2025), IF : 8.5 (2023 JCR)
  - ✓ Composites Part : B, 304, 112693 (2025), IF : 12.7 (2023 JCR)
  - ✓ Materials & Design, 103, 796-808 (2025), IF : 7.6 (2023 JCR)
  - ✓ Materials Letters, 396, 131996 (2023), IF : 11.2 (2022 JCR)
  - ✓ Advanced Composited and Hybrid Materials, 6(5), 182 (2023), IF : 20.1 (2022 JCR)
  - ✓ Nano Research, 11, 2190-2203 (2018), IF : 9.9 (2022 JCR)
- Research Areas
  - ✓ Semiconductor Package Reliability/Mechanics Performance Evaluation/Analysis Technology
  - ✓ Next-generation Semiconductor Package Process Technology Development
  - ✓ Terahertz Wave-based Material Characterization Technology Development
  - ✓ Terahertz Wave-based Real-time Semiconductor Package Inspection Technology Development
  - ✓ **Advanced Composite Materials Precision Analysis and Multi-functional Composite Structure Design Research**
  - ✓ **Artificial Intelligence Application Technology Development**
  - ✓ **Printed Electronics Technology Development**

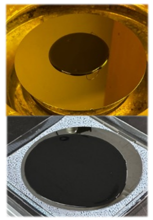
- FABRICATION & PROCESS



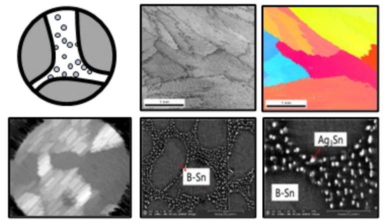
Design



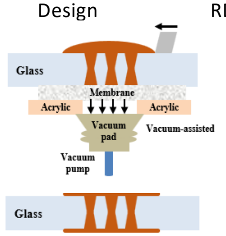
RDL patterning



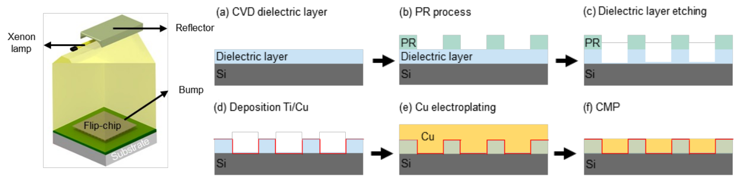
EMC molding



Solder ball & Cu pillar

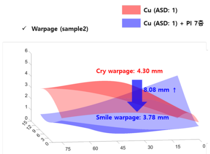


TGV/Interposer

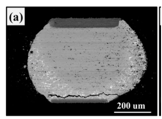


IPL bonding / Flux-less bonding / Hybrid bonding

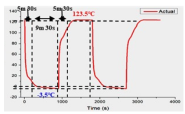
- Reliability



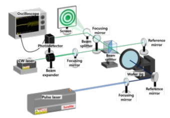
Warpage



Solder joint reliability
(creep, IMC, fatigue)

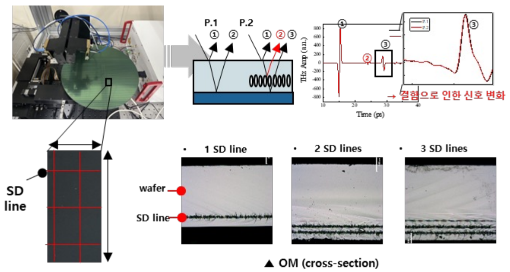


TC/B-Hast/Aging



Adhesion

- Inspection



EMC thickness, PKG warpage, chip alignment inspection / Stealth diced line inspection

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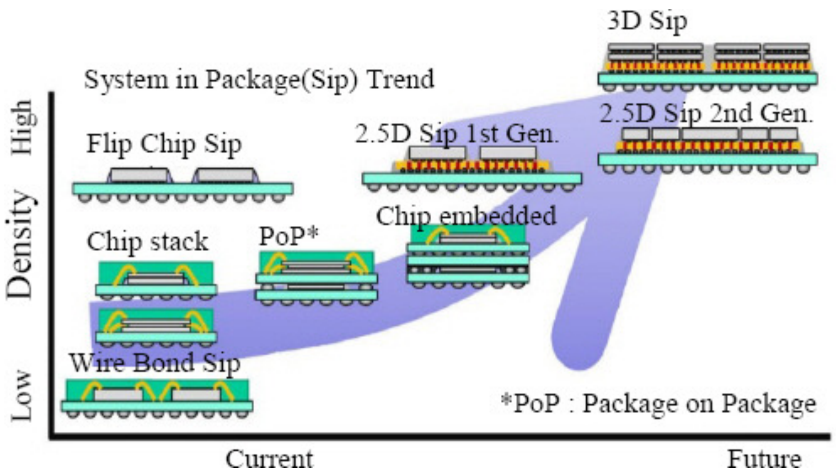
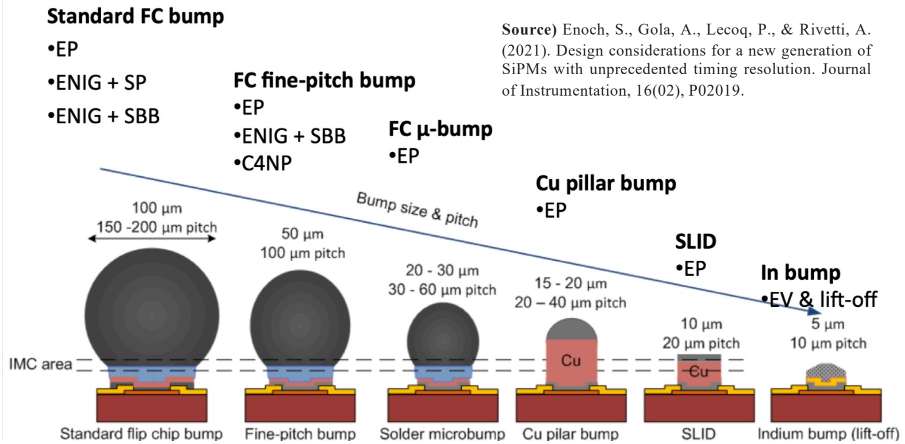
❖ Semiconductor Packaging Evolution: Toward High Integration



▲ Package type trend

Source) Lau, J. H. (2010, December). Evolution and outlook of TSV and 3D IC/Si integration. In *2010 12th Electronics Packaging Technology Conference* (pp. 560-570). IEEE.



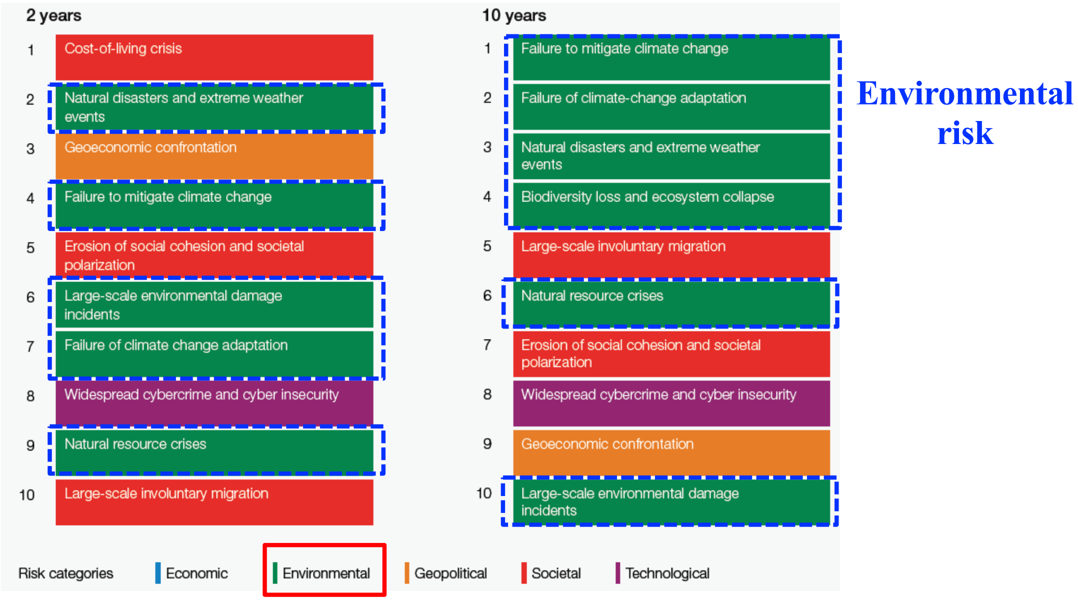
Source) Enoch, S., Gola, A., Lecoq, P., & Rivetti, A. (2021). Design considerations for a new generation of SiPMs with unprecedented timing resolution. Journal of Instrumentation, 16(02), P02019.

▲ Interconnection trend

- A highly integrated semiconductor package product is required.
- Package and interconnection type with various structures and sizes are being developed.
- The interconnection processes is also changing according to the package trend.

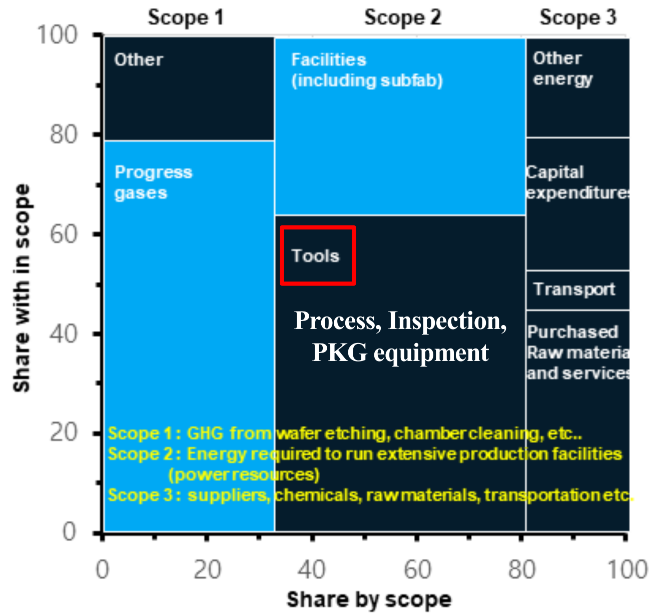
❖ Sustainability in Packaging: Energy and CO_2 Emission Concerns

Source) World Economic Forum, Global Risks, Perception Survey 2022-2023



▲ **Global Short-term and Long-term Risk Rankings**

Source) McKinsy & Company https://www.mckinsey.com

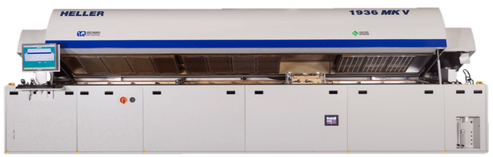


▲ **CO_2 Emission Proportion in Semiconductor Manufacturing Process**

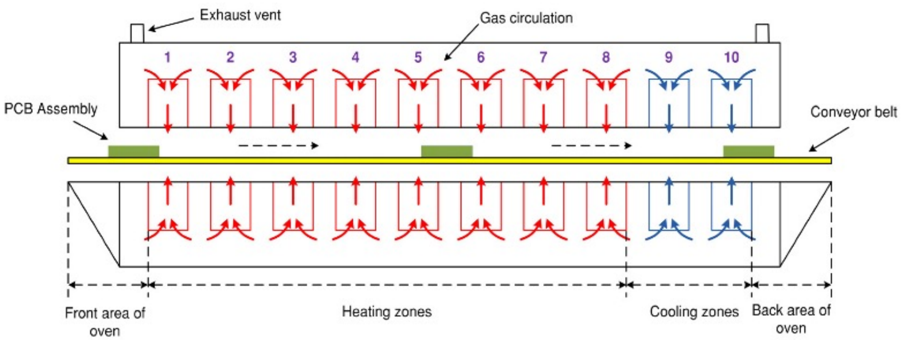
- Energy consumption in semiconductor manufacturing is identified as a critical global risk factor
- CO_2 emissions primarily come from process gases, manufacturing tools, and facility operations
- The industry urgently needs energy-efficient manufacturing technologies to meet sustainability goals

❖ Conventional Interconnection: Mass Reflow Process

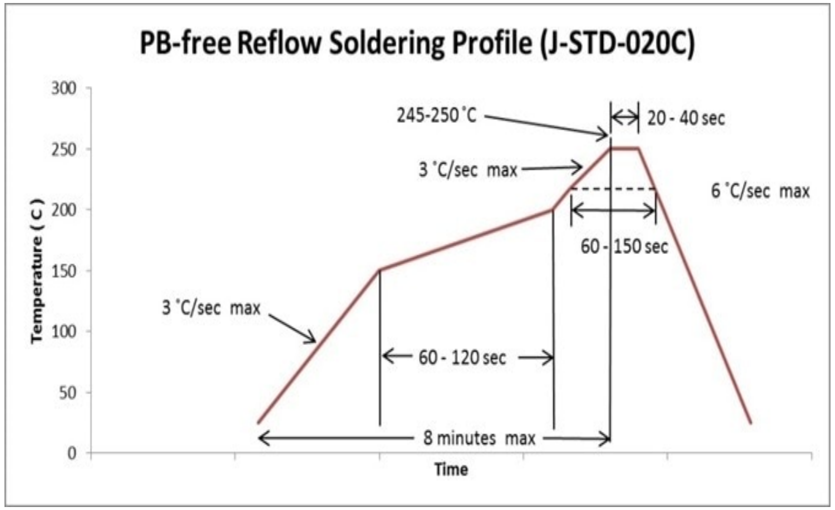
Source) Heller Industries, Inc.



Source) Guo, Y., Liu, M., Yin, M., & Yan, Y. (2022). Reliability sensibility analysis of the PCB assembly concerning warpage during the reflow soldering process. *Mathematics*, *10*(17), 3055.



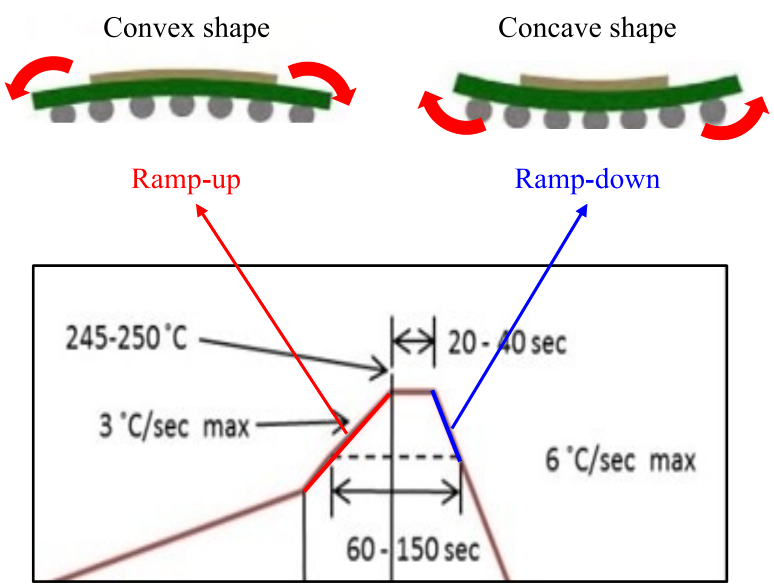
▲ **Industrial reflow soldering equipment**



▲ **JEDEC J-STD-020C Reflow Profile**

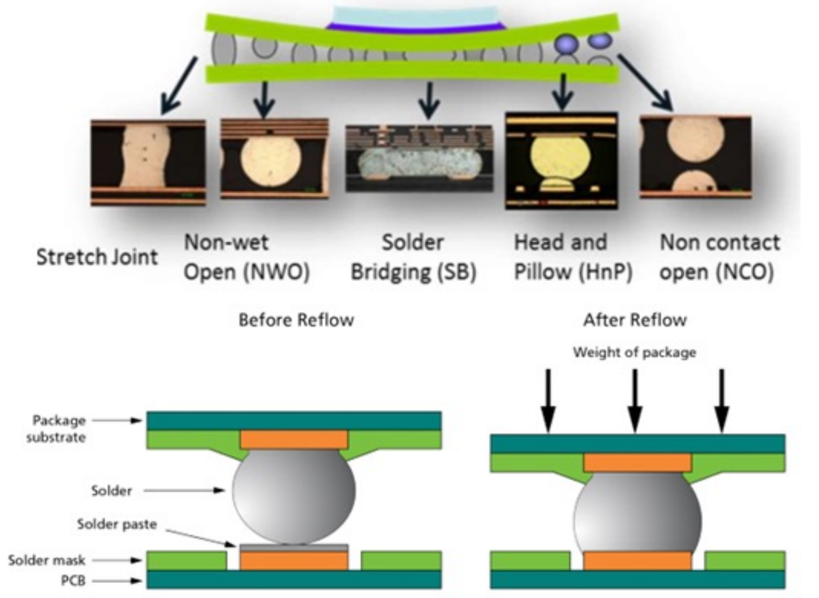
- Mass reflow is most used interconnection method in many application such as flip-chip die attach, ball mounting, and surface mount technology.
- Reflow machine consists of zones of different temperatures.
- The temperature profile follows JEDEC standard.

❖ Challenges of Mass Reflow: Package Warpage



▲ **Warpage in reflow process**

Source) SMT-007magazine, Micron report



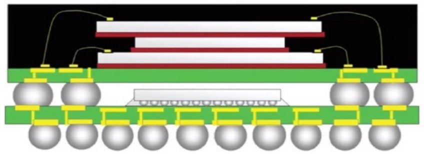
▲ **Solder joint reliability issues from warpage**

- The heat is applied to the entire packages during long process time in reflow zone.
- Therefore, warpage occurs due to the difference CTE between silicon chip and PCB during mass reflow.

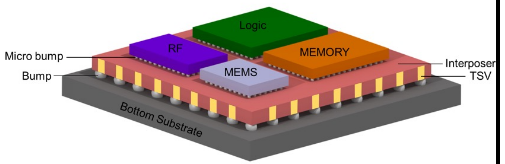
❖ Advanced Packages: More Vulnerable to Warpage in Mass Reflow

Advanced PKG characteristics
- Ultra-thin substrates/dies
- Heterogeneous materials
- Complex 3D architecture
- Larger package size

Source) JCET Group

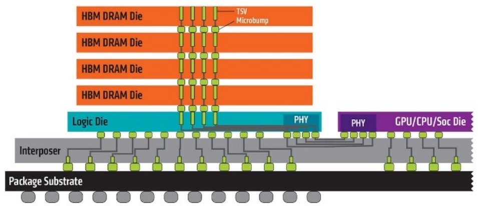


▲ **PoP**



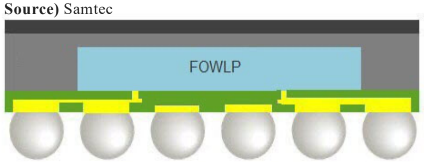
▲ **SiP**

Source) AMD



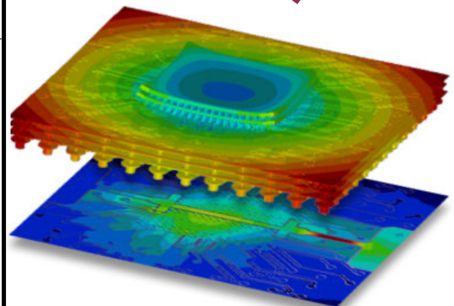
▲ **HBM (2.5D package)**

Source) Samtec



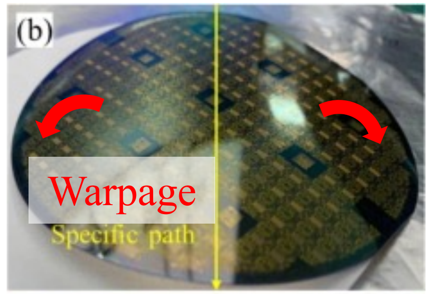
▲ **FO-WLP**

POP: Package on package
SiP : System in package
HBM :High band-width package
FO-WLP : Fan-out wafer level package



▲ **Thermo-mechanical reliability issue**

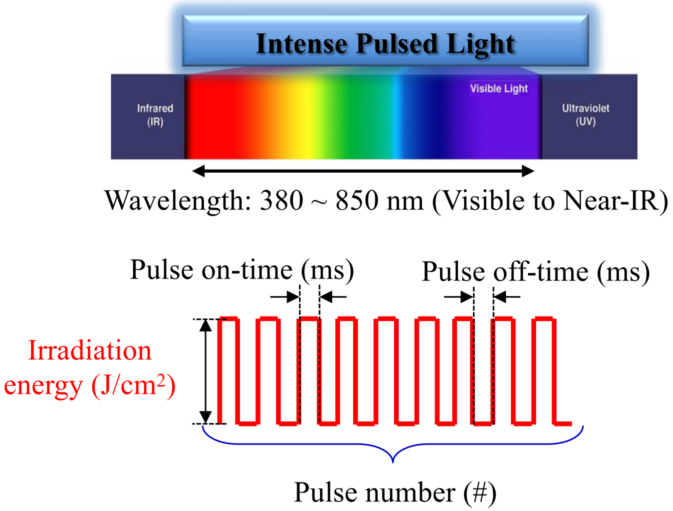
Why more vulnerable?
- **Larger CTE mismatch**
- **Less mechanical strength**
- **Multiple interfaces**



Source) Lee, H. J., Park, S. M., & Park, S. J. (2016). Minimization of warpage for wafer level package using response surface method. *International Journal of Precision Engineering and Manufacturing*, *17*, 1201-1207.

- Advanced packages (FO-WLP, PoP, HBM, SiP) are inherently more susceptible to warpage due to their complex structure.
- The combination of ultra-thin components and heterogeneous materials amplifies warpage in mass reflow.
- Conventional mass reflow becomes increasingly problematic as package complexity increases.

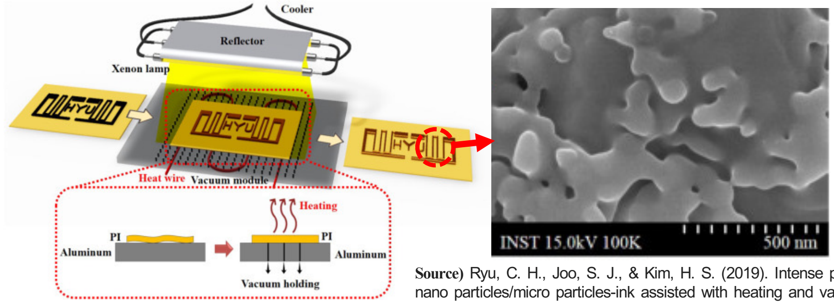
❖ Intense pulsed light (IPL) Technology and Applications



▲ Schematic of IPL pulse

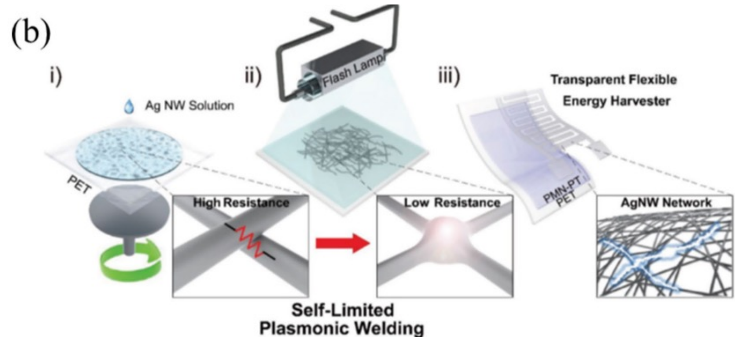
IPL applications

1. Metal particles sintering: ultra-fast, low-temperature process



Source) Ryu, C. H., Joo, S. J., & Kim, H. S. (2019). Intense pulsed light sintering of Cu nano particles/micro particles-ink assisted with heating and vacuum holding of substrate for warpage free printed electronic circuit. *Thin Solid Films*, *675*, 23-33.

2. Nanowire welding: selective heating, minimal substrate damage

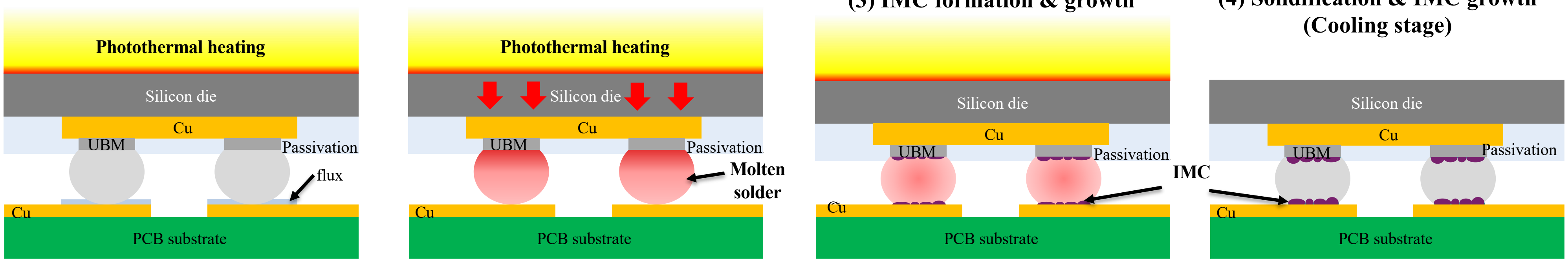


Source) Park, J. H., Hwang, G. T., Kim, S., Seo, J., Park, H. J., Yu, K., ... & Lee, K. J. (2017). Flash-induced self-limited plasmonic welding of silver nanowire network for transparent flexible energy harvester. *Advanced Materials*, *29*(5), 1603473.

❖ Mechanism of Intense Pulsed Light (IPL) Bonding Process

Source) Ju, Y. M., Ryu, S. U., Park, J. W., & Kim, H. S. (2025). Ultra-Millisecond Flip-Chip Bonding Process via Intense Pulsed Light Irradiation. *ACS Applied Materials & Interfaces*.

(1) Initiation of IPL irradiation (T < 217°C) | **(2) Solder liquidation (T > 217°C)** | **(3) IMC formation & growth** | **(4) Solidification & IMC growth (Cooling stage)**



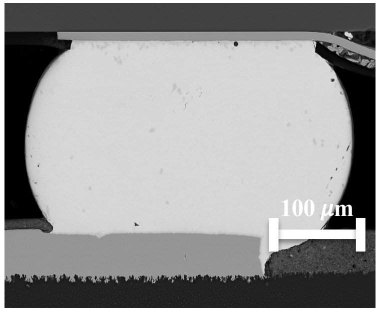
(1)
- Silicon absorbs IPL energy
- Rapid photo-thermal conversion

(2)
- SAC305 melting point reached

(3)
- Cu-Sn interdiffusion
- IMC (Cu_6Sn_5) layer formation

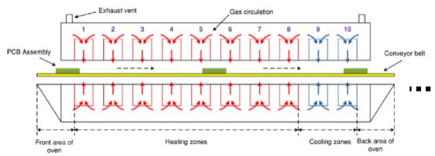
(4)
- Rapid cooling
- Controlled IMC thickness

- During IPL bonding process, the heat generated by photothermal effect in silicon die is rapidly transferred to solder bump.
- The ultra-fast heating enables melting and bonding within milliseconds, minimizing thermal exposure.
- Controlled IMC formation at the interface ensures reliable interconnection with minimal thickness.



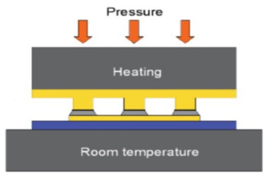
▲ Solder joint after IPL bonding process

❖ Comparison of Interconnection Methods: Limitations and IPL Advantages



Convection Reflow

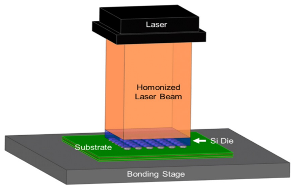
- ✓ High power consumption
- ✓ Long process time



Source) Li, Junhui, et al. (2020)

Thermo-Compression

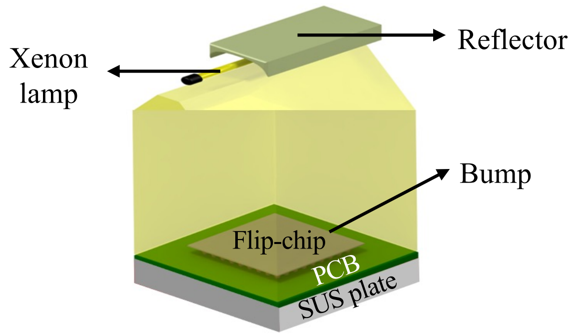
- ✓ High cost (Equipment & Process)
- ✓ Long process time



Source) JANG et al. (2020)

Laser Assisted bonding

- ✓ High cost (Equipment & Process)
- ✓ Limited spot size



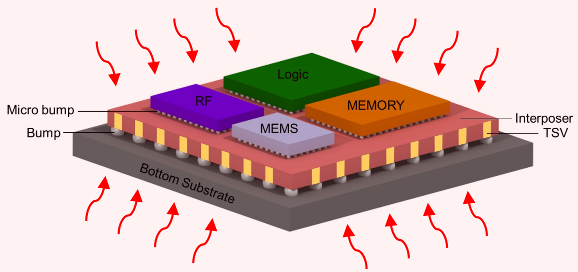
Intense Pulsed Light process Benefits

- ✓ Ultra-fast process (milliseconds)
- ✓ Large area batch processing
- ✓ Low temperature & energy efficient
- ✓ Minimal warpage & IMC control
- ✓ Cost-effective solution

- Various interconnection methods have been developed to address the limitations of conventional reflow
- Each alternative method has its own drawbacks limiting widespread adoption
- IPL bonding combines the advantages of existing methods while overcoming their limitations

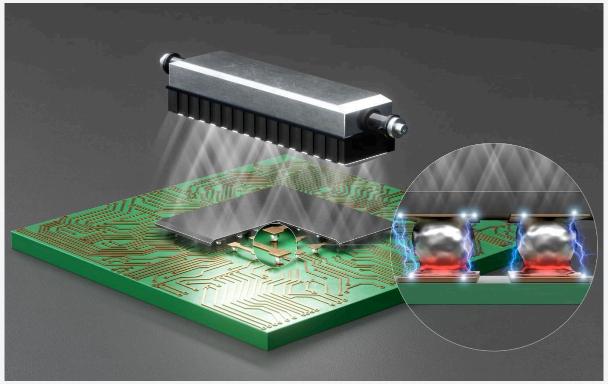
❖ Research Objective

Conventional Mass Reflow



- ✓ High power consumption (Max. temp 250℃, 5-8 min duration)
- ✓ Long process time (60-150 s above liquidus)
- ✓ Heat applied to entire package
- ✓ Severe warpage issues
- ✓ Excessive IMC growth (>5 μm)

IPL bonding process

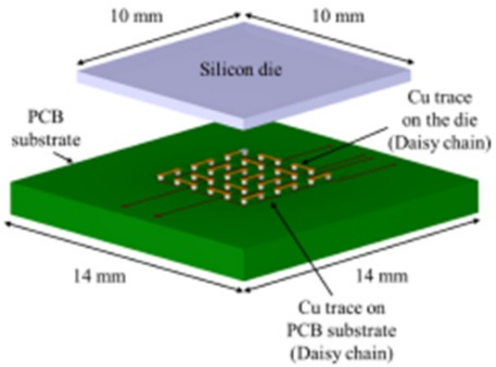


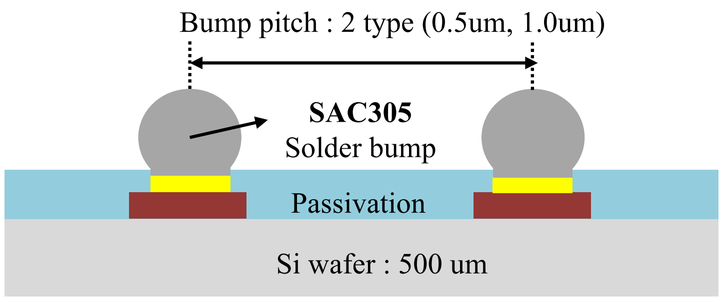
- ✓ Low energy consumption
- ✓ Ultra-fast process (total process time < 1 s)
- ✓ Selective heating via photothermal effect
- ✓ Minimal warpage
- ✓ Controlled IMC thickness (<1 μm)

- The objective of this study is to demonstrate IPL bonding as a viable alternative to conventional mass reflow
- Key focus: Process optimization, reliability assessment, and scalability for flip-chip applications
- Goal: Achieve superior bonding quality with reduced energy, time, and thermal damage

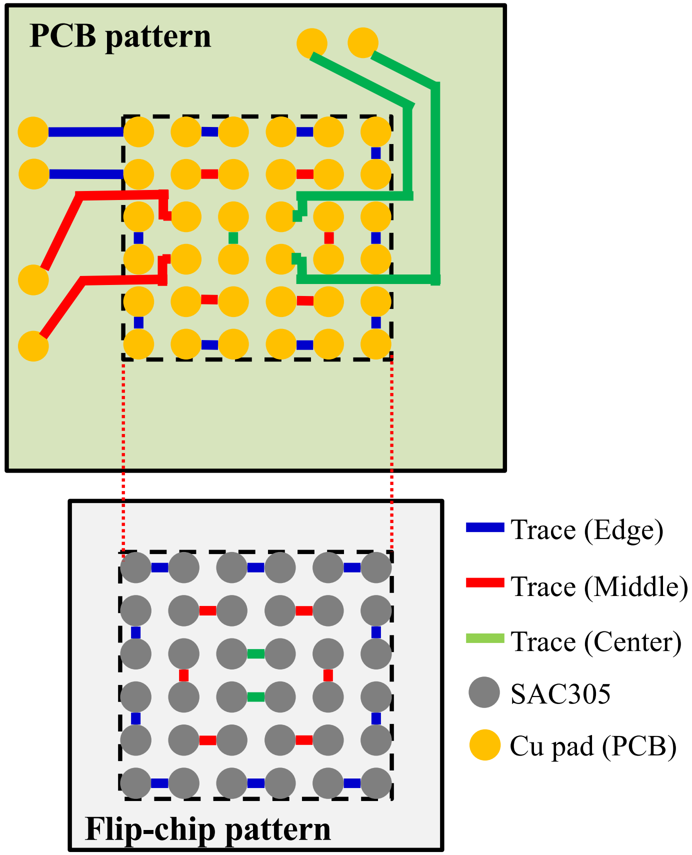
Contents

❖ Flip-chip Test Sample Preparation



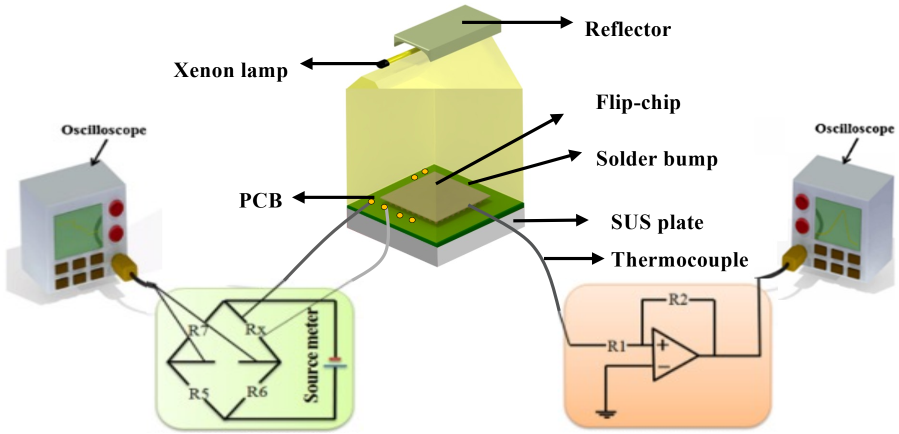


▲ **Flip-chip sample structure**



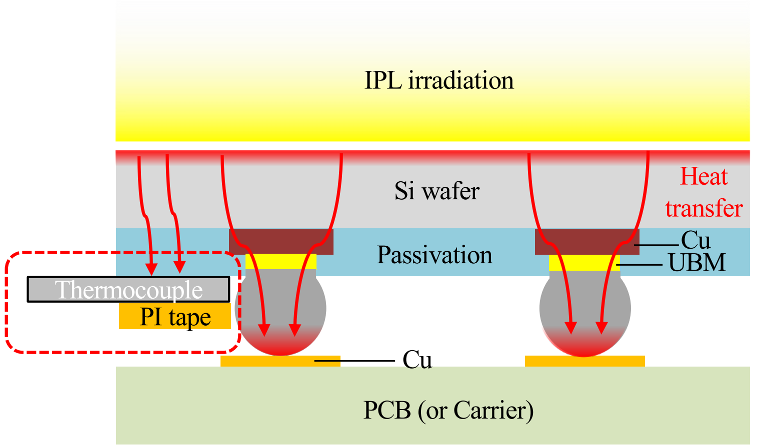
- SAC305 (Sn-3.0Ag-0.5Cu) was selected as the most widely used lead-free solder.
- Three daisy chain patterns enable location-specific resistance monitoring during bonding.

❖ In-situ Temperature and Resistance Monitoring Systems

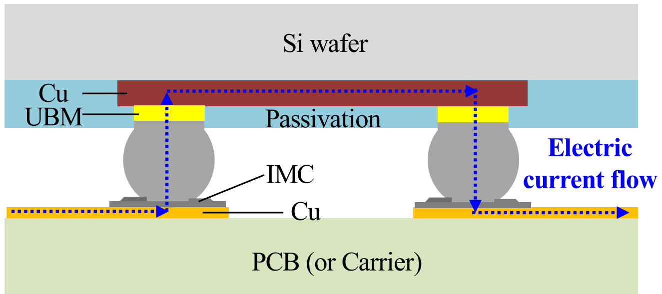


▲ Resistance monitoring system (Wheatstone bridge)

▲ Temperature monitoring system (OP-AMP & Thermocouple)



▲ Measure the temperature



▲ Measure the resistance

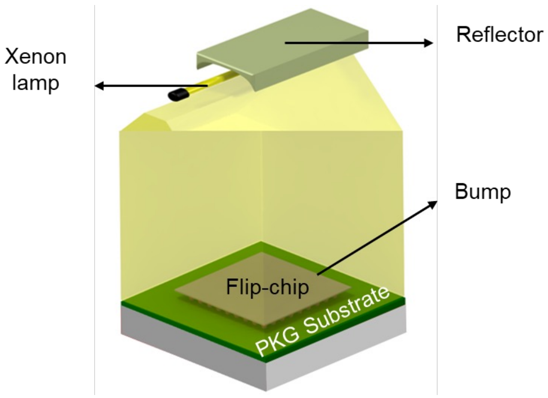
- Dual in-situ monitoring system provides comprehensive process data during IPL bonding.
- Temperature measurement tracks thermal profile precisely
- Resistance monitoring through daisy chain detects exact melting and solidification moments.

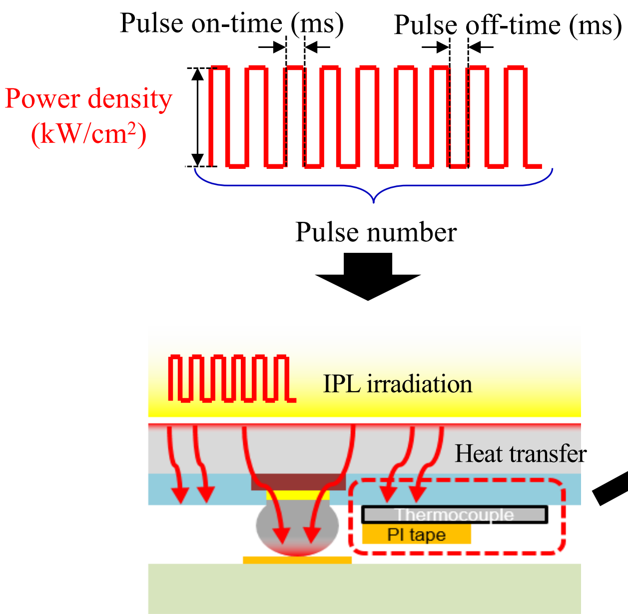
❖ IPL Process Parameters and Control

<Appendix : Parametric Exp.>

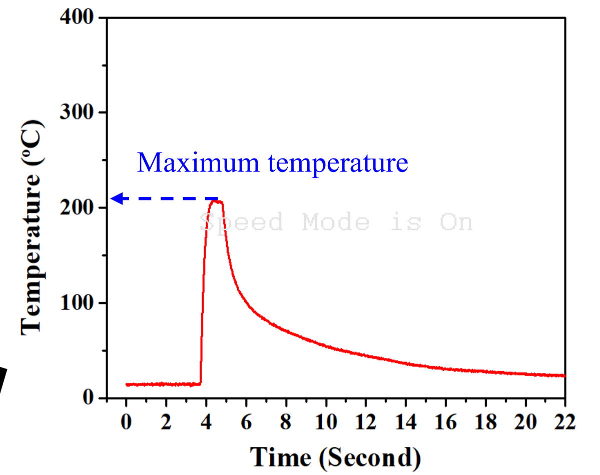
IPL process parameters

- Frequency
- On/Off time
- Pulse number
- Power





Example)

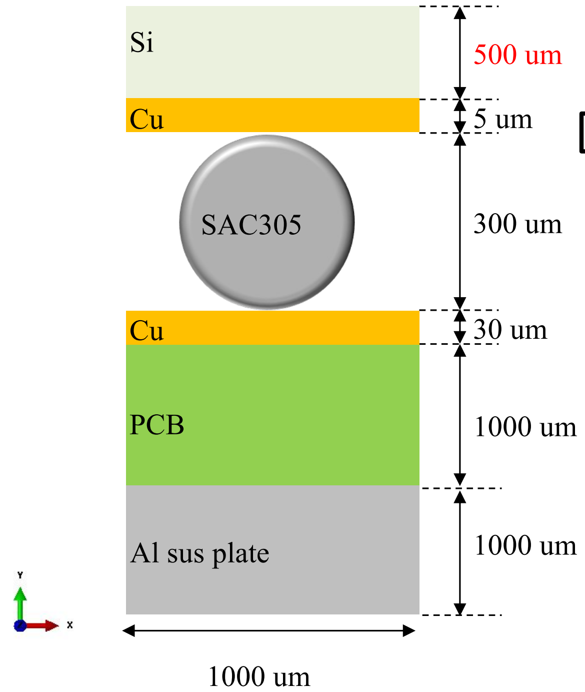


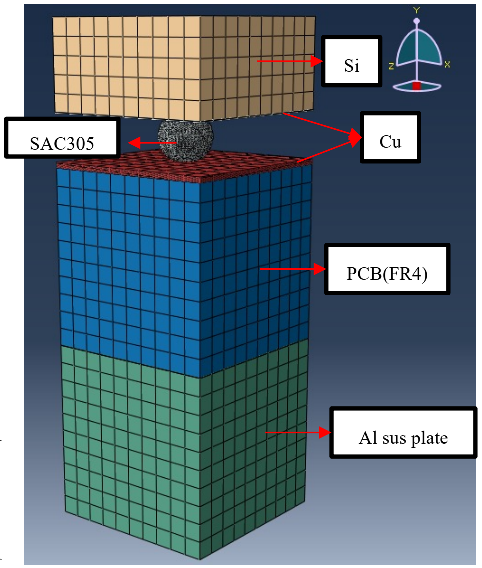
▲ **Temperature profile during IPL bonding**

- The IPL energy can be controlled under conditions such as pulse on/off time, pulse number, power and frequency.

❖ Heat Transfer Simulation Model

Part – 3D





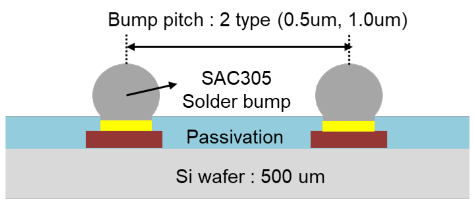
*Ti (100 nm) : Relatively very thin film, Ti layer is negligible.

*Passivation layer (10 um) : very low thermal conductivity, Passivation layer is negligible.

Materials

<Appendix : Governing equation>

Materials	Density [kg/m^3]	Heat capacity [J/kg·K]	Thermal conductivity [W/m·K]
Si	2330	790	98.9
Cu	8993	397	393
SAC305	7380	230	58
PCB(FR4)	1800	1100	0.29
Al	2720	905	170
Polyimide (Passivation)	1390	1150	0.52



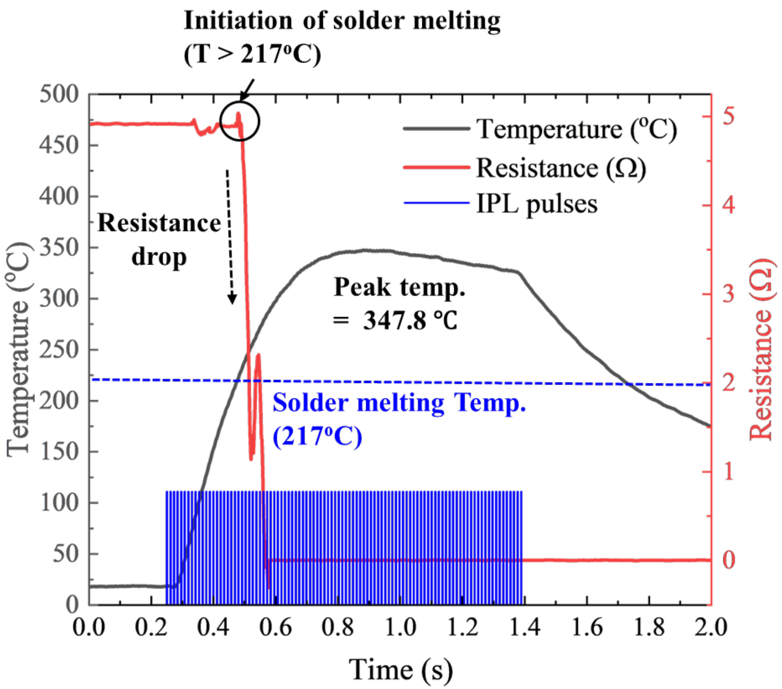
- The heat transfer modeling was carried out using Abaqus CAE, and the properties (density, heat capacity, thermal conductivity) of each layer were referenced from relevant literature.

Contents

❖ In-situ Temperature and Resistance Monitoring of IPL Flip-chip Bonding Process

<Appendix : 1. Pulse On-time>
<Appendix : 2. Frequency>

▣ Representative in-situ monitoring results (On-time : 1.5 ms (= **Irradiation energy : 0.933 kW/cm²**), Frequency : 100 Hz, and Pulse number : #100)

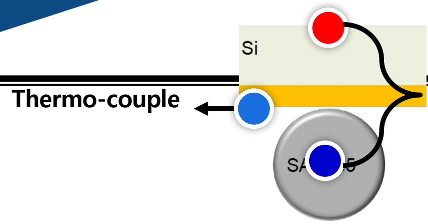


Finding

- Bonding completed at ~217°C (resistance drop)
- But temperature keeps rising to ~350°C
- Excessive heating after bonding completion

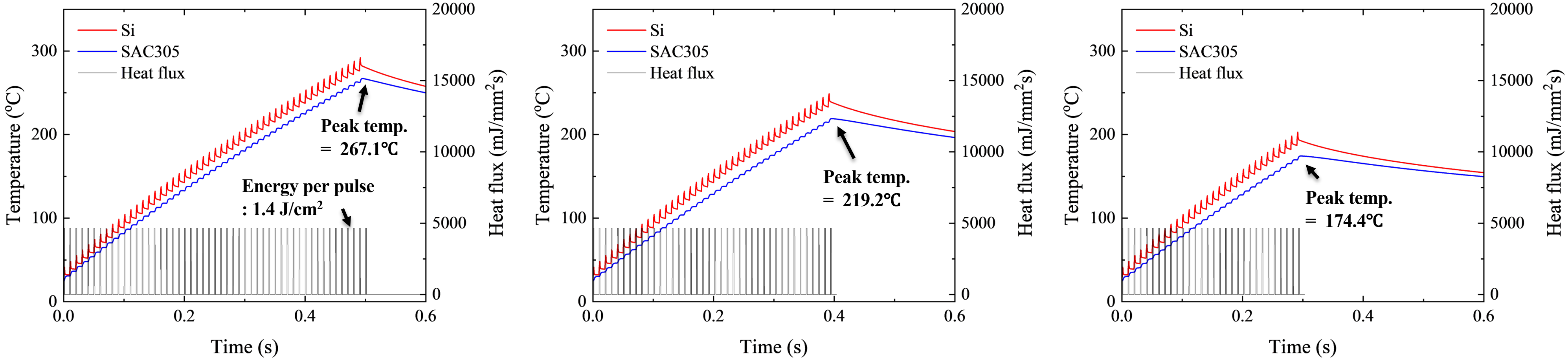
Objective

- Find minimum pulses for reliable bonding
- Target : Peak temperature ~ 220°C (Solder melting point : 217°C)



❖ Thermal Simulation for Pulse Number Optimization

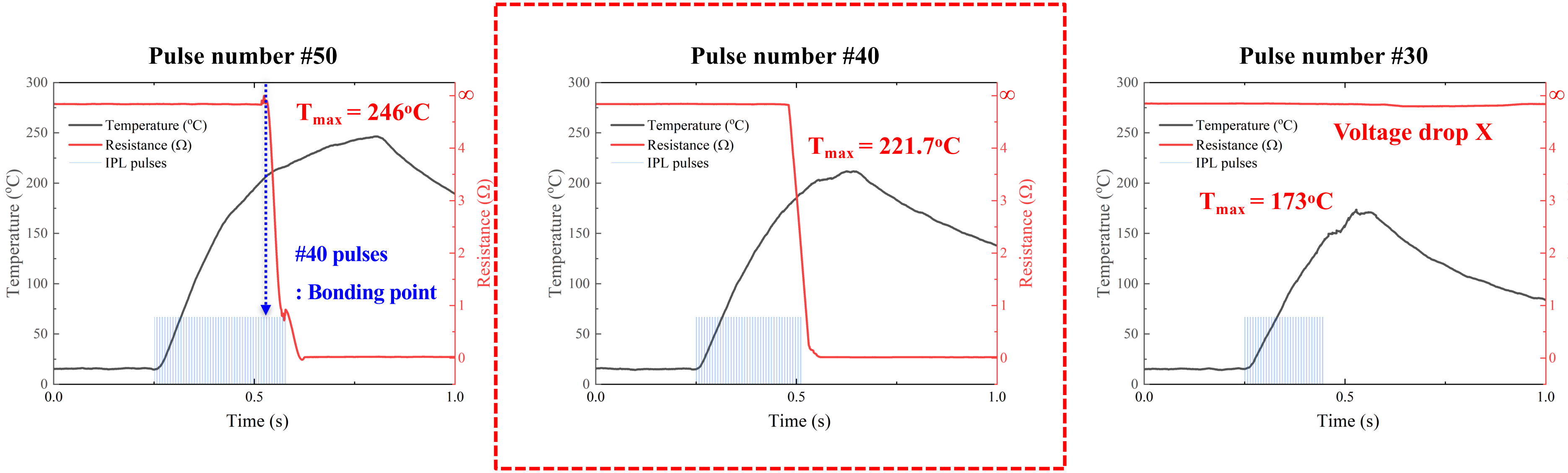
▣ Pulse number optimization study **(simulation results)**



- Thermal simulation was conducted to predict optimal pulse number for IPL flip-chip bonding process.
- Simulation results predicted that 30 pulses would be insufficient (174˚C < 217˚C melting point), while 50 pulses would cause excessive heating (267˚C).
- Based on simulation, 40 pulses was identified as the theoretical optimum, achieving 219˚C, above the melting point, with minimal heat excess.

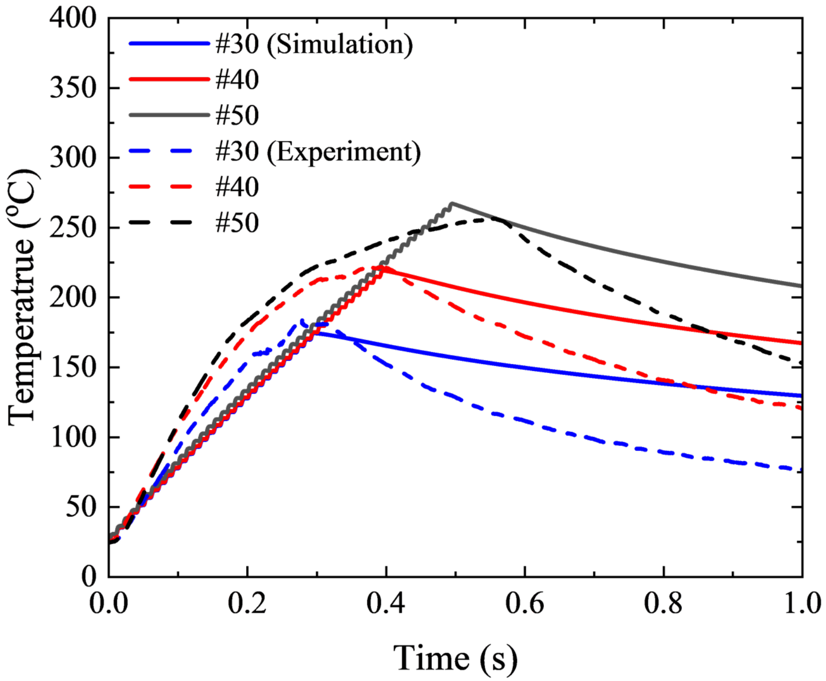
❖ In-situ Temperature and Resistance Monitoring of IPL Flip-chip Bonding Process

▣ Pulse number optimization study **(Experiment)**

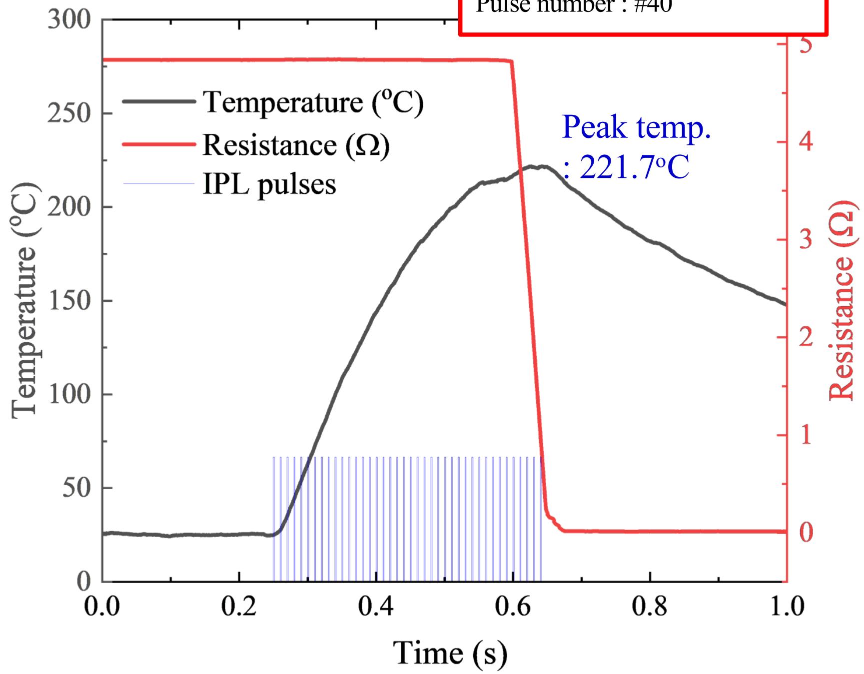


- Experimental validation was performed based on simulation predictions using in-situ temperature and resistance monitoring.
- The experimental results confirmed simulation predictions: 30 pulses failed to achieve bonding (173°C), while 40 pulses successfully achieved bonding at 221°C.

❖ Validation of Simulation Model with Experimental Results



Optimized IPL condition
On-time : 1.5 ms
Off-time : 8.5 ms
Power density : 0.933 kW/cm^2
Pulse number : #40

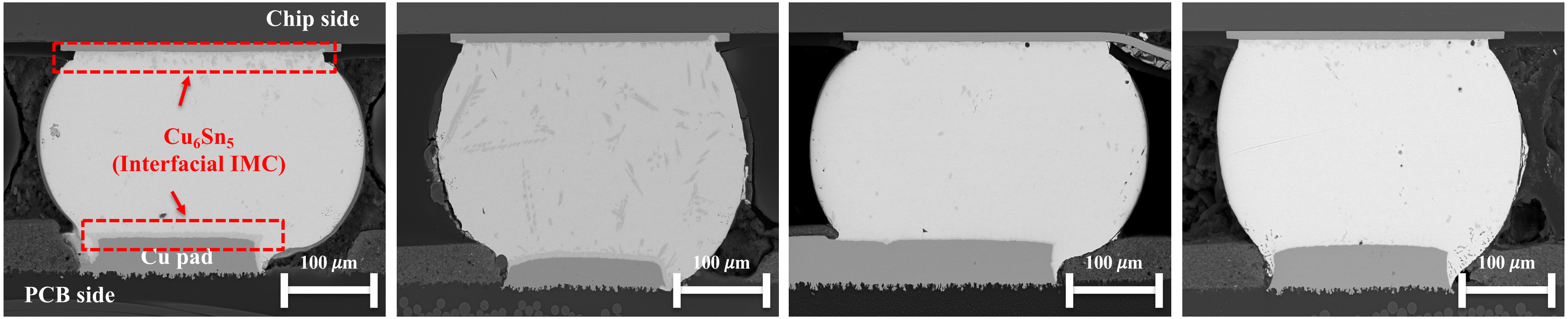


- Excellent correlation between simulation and experimental results validates the thermal model's accuracy.
- The simulation-guided optimization successfully identified 40 pulses as optimal, achieving reliable bonding at the lowest temperature (221.7°C) while avoiding both under-heating and thermal damage.

❖ Cross-sectional SEM image of flip-chip package solder joint

▣ IMC(Intermetallic compound) thickness and microstructures

Reflow (250 °C, 300s)	Pulse number: 100	Pulse number: 50	Pulse number: 40



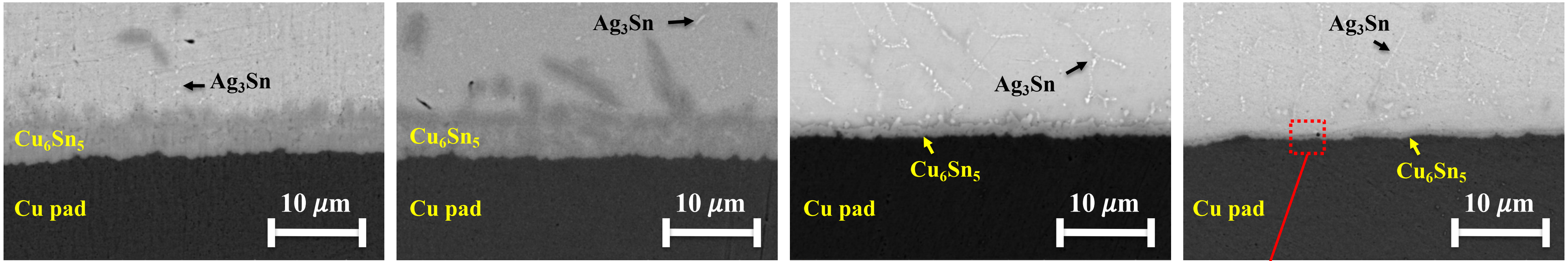
Peak temp.: 250°C	Peak temp.: 347.8°C	Peak temp.: 246°C	Peak temp.: 221.7°C

- SEM analysis confirms successful solder joint formation for all IPL conditions tested, with no visible defects or voids.

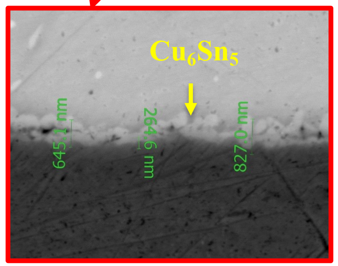
❖ Cross-sectional SEM image of flip-chip package solder joint

▣ IMC(Intermetallic compound) thickness and microstructures

Reflow (250 °C, 300s)	Pulse number: 100	Pulse number: 50	Pulse number: 40



Reflow (250 °C, 300s)	Pulse number: 100	Pulse number: 50	Pulse number: 40
Peak temp.: 250°C IMC thickness : ~6 μm	Peak temp.: 347.8°C IMC thickness : ~6 μm	Peak temp.: 246°C IMC thickness : ~2 μm	Peak temp.: 221.7°C IMC thickness : ~800 nm

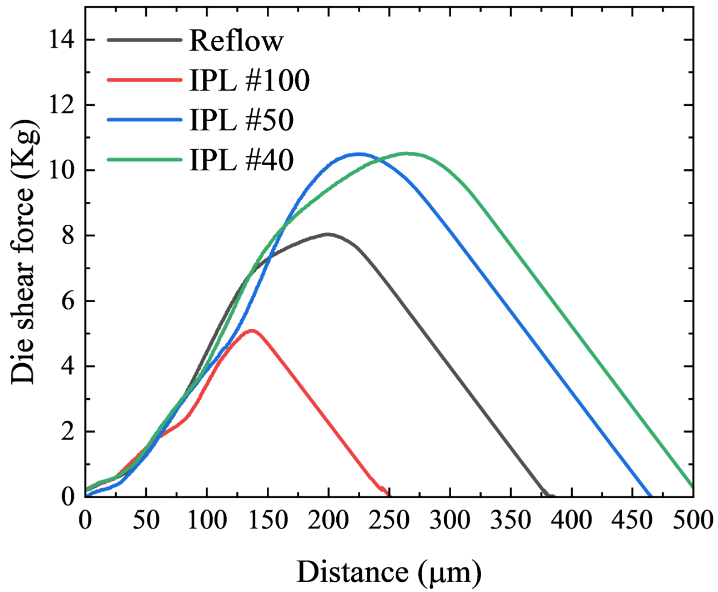


- IMC thickness analysis reveals dramatic differences: Reflow and 100-pulse IPL (~6 μm) vs. optimized 40-pulse IPL (~800 nm).
- The ultra-thin IMC achieved with 40 pulses results from precise thermal control - sufficient heat for bonding but minimal time for excessive intermetallic growth.

❖ Mechanical Reliability Evaluation by Die Shear Test

<Appendix : Die shear test configuration>

▣ Results of die shear test

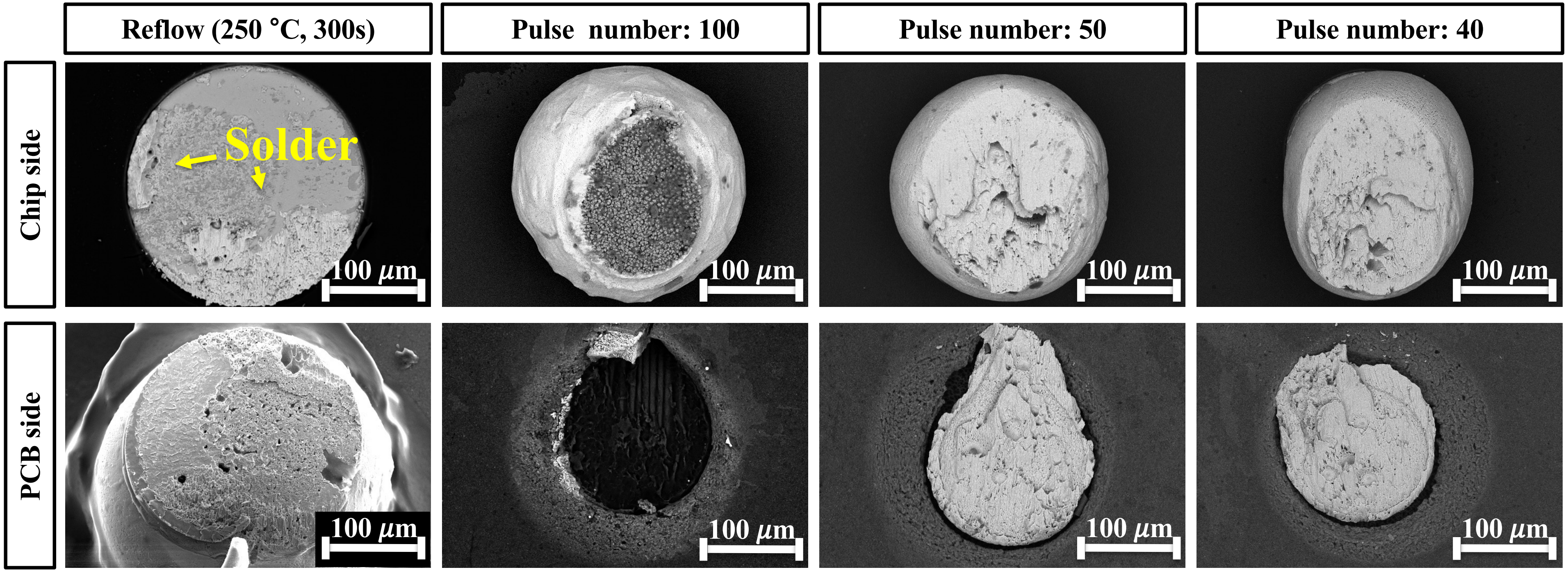


Sample	Process		Max die shear force (kg)	IMC thick. (um)
SAC305 PKG (pitch: 1000 um, thick: 500 um)	Mass Reflow		8.028	6
	IPL bonding (Pulse number)	#40	10.514	0.8
		#50	10.491	2
		#100	5.09	6

- In the case of IPL #50 and #40 specimens, a relatively 30% higher shear force was measured compared to the reflow specimens.
- On the other hand, the IPL #100 specimen showed a comparatively lower shear force.

❖ Mechanical Reliability Evaluation by Die Shear Test

▣ Fracture analysis



IMC fracture
(Thick IMC → Brittle behavior)

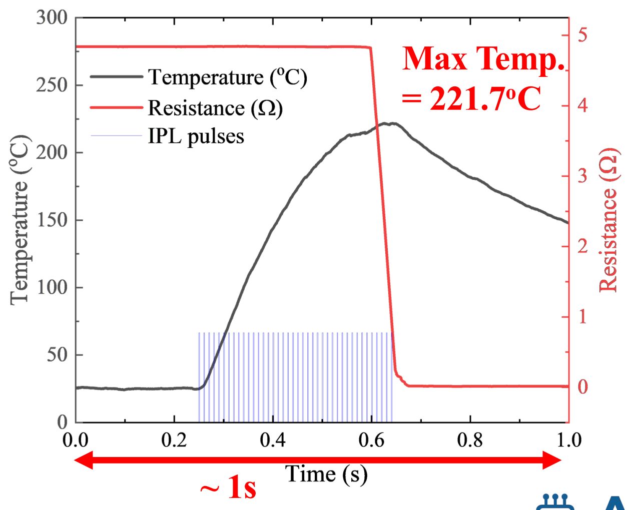
PAD lift
(Thermal damage to PCB)

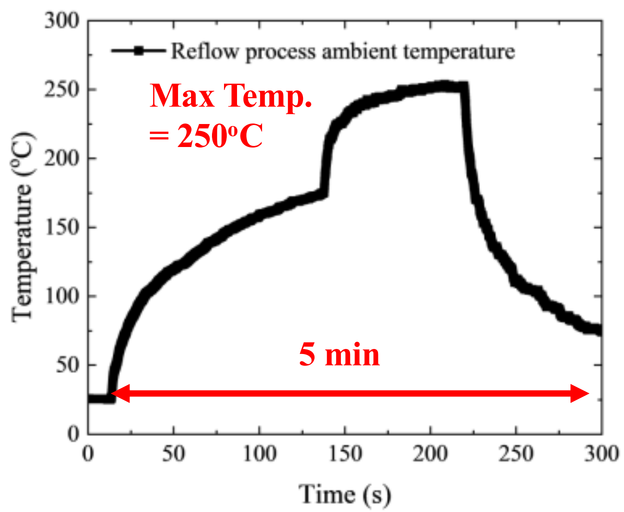
Solder bulk fracture
(Ductile fracture)

Die shear force ↑

❖ IPL vs Reflow Process Comparison: Temperature Profile & Processing Time

Item	IPL (Intense Pulsed Light)	Reflow (Conventional Hot Air)
Processing Method	Instantaneous High-Intensity Light	Continuous Hot Air Heating
Maximum Temperature	221.7°C	250°C
Processing Time	1~2 seconds (40 pulses)	5 minutes (300 seconds)
Temperature Rise Rate	Ultra-high speed	Gradual





❖ IPL vs Reflow Process Comparison: Energy Consumption

	IPL (Intense Pulsed Light)	Reflow (Conventional Hot Air)
Peak Power	933W	2,700W
Average Power	140W	1,890W
Processing Time	0.4 seconds	300 seconds
Energy Consumption	0.056 kWh	0.16 kWh
Energy Efficiency	$\boxed{\text{3x superior}}$	Baseline

Note: *Energy consumption values are estimated based on equipment specifications and typical operating conditions. Actual values may vary depending on specific equipment models and operating parameters.*

IPL Conditions:
- On-time: 1.5 ms per pulse
- Off-time: 8.5 ms per pulse
- Power density: 0.933 kW/cm²
- Pulse number: 40 pulses
- Processing area: 1 cm² (10mm × 10mm chip)
- Total processing time: 0.4 seconds
- Peak temperature: 221.7°C

Reflow Conditions:
- Power rating: 2.7 kW (15A @ 220V)
- Processing time: 5 minutes (300 seconds)
- Average power utilization: 70% (temperature profile consideration)
- Peak temperature: 250°C

[1] IPL Energy = Peak Power × Total On-time
= 933W × (40 × 1.5ms) = 933W × 0.06s = 0.056 kWh

[2] Reflow Energy = Average Power × Processing Time
= (2.7kW × 0.7) × (5/60)h = 1.89kW × 0.083h = 0.16 kWh

Contents

Thank you

❖ Parametric Investigation of IPL Bonding Process

<Back>

Objectives

- **Optimize IPL parameters for damage-free bonding**
- **Minimize process time while ensuring reliability**

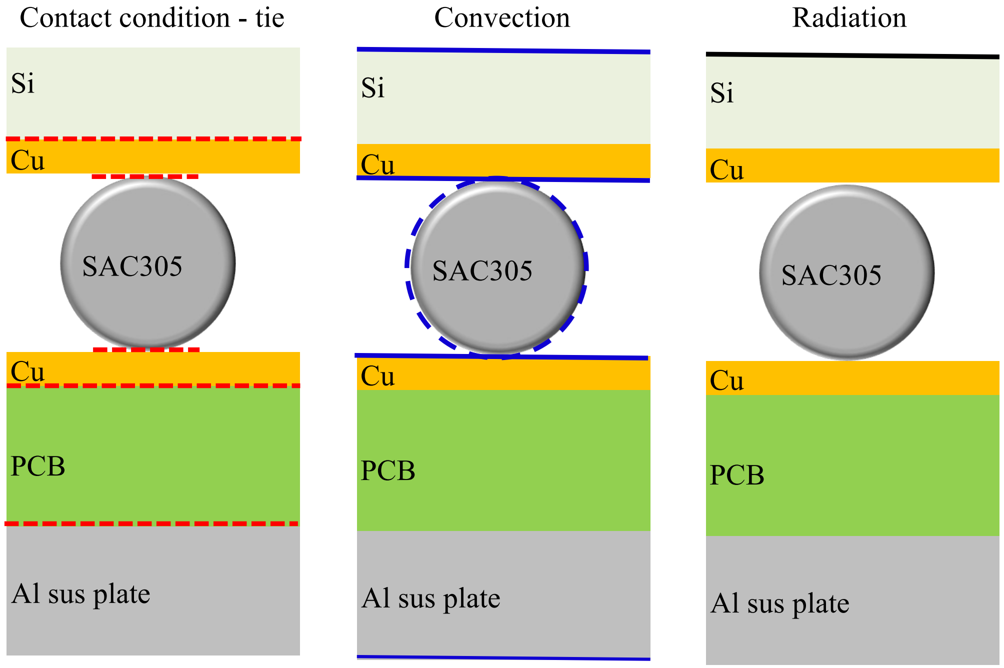
Case	Variable	On-time (ms)	Frequency (Hz)	Pulse number (counts)	Irradiation energy (J/cm^2)
1	On-time	1	100	100	1.4
2		1.5	100	100	1.4
3		2.25	100	100	1.4
4	Frequency	1.5	100	100	1.4
5		1.5	90	100	1.4
6		1.5	80	100	1.4
7	Pulse number	1.5	100	50	1.4
8		1.5	100	40	1.4
9		1.5	100	30	1.4

Table 1. Experimental conditions of IPL bonding process

❖ Heat Transfer Simulation Model

<Back>

Boundary condition



Assumption) The light absorption rate of silicon was assumed to be 50%.

$*\varepsilon_{SB}: 5.76 * 10^{-8}\ (Wm^{-2}K^{-4})$

$*\sigma_{\text{emissivity}}: 0.6\ (silicon)$

$*h: 30\ (Wm^{-2}K^{-1})$ (Natural cooling, free − air)

Governing equations

- Conduction

$$q = -kA\frac{dT}{dn}$$

$k: thermal\ conductivity\ (Wm^{-1}K^{-1})$

$A: cross-sectional\ area (m^2)$

$\frac{dT}{dn}: temperatreu\ gradient (km^{-1})$

- Convection

$$q = hA(T_{surface} - T_{\infty})$$

$h: heat\ transfer\ coefficient\ (Wm^{-2}K^{-1})$

$T_{surface}: temperature\ of\ surface\ (K)$

$T_{\infty}: temperature\ of\ ambient\ (K)$

$A: Surface\ area (m^2)$

- Radiation

$$q = \varepsilon_{SB}\sigma A(T_{surface}^4 - T_{\infty}^4)$$

$\varepsilon_{SB}: Stefan-Boltzman\ constant\ (Wm^{-2}K^{-4})$

$T_{surface}: temperature\ of\ surface\ (K)$

$T_{\infty}: temperature\ of\ ambient\ (K)$

$A: Surface\ area (m^2)$

$\sigma: emissivity\ of\ the\ surface$

$$\rho c_p \frac{\partial T}{\partial t} = \nabla \cdot (k\nabla T) + q$$

$\rho: density\ (kgm^{-3})$

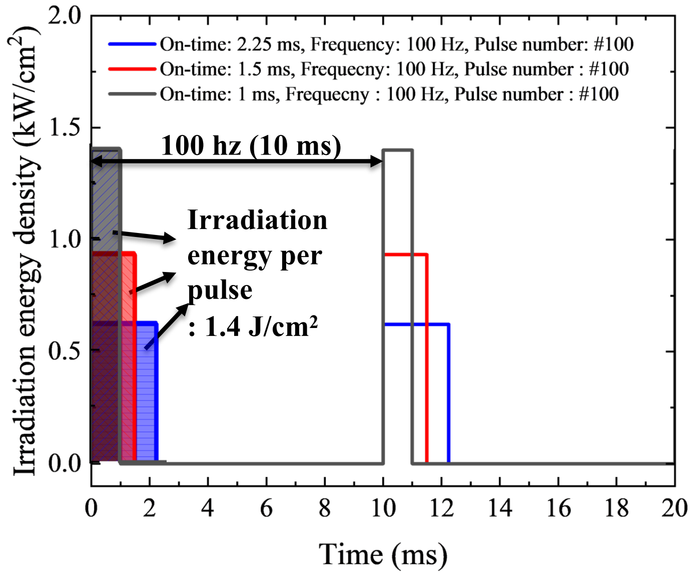
$C_p: specific\ heat\ capacity\ (Wm^{-2}K)$

❖ Effect of Pulse On-time on Temperature Profile

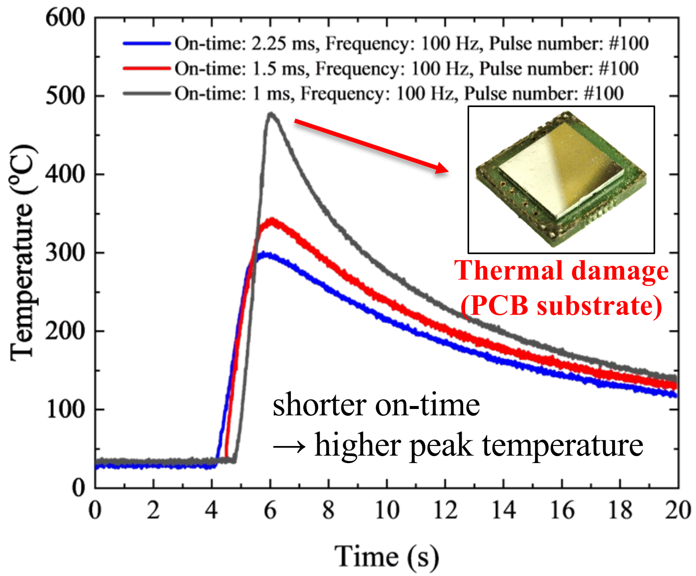
<Back>

▣ IPL parameter with On-time

✓ **On-time (2.25 / 1.5 / 1 ms)**



✓ **Temperature profiles during IPL bonding**



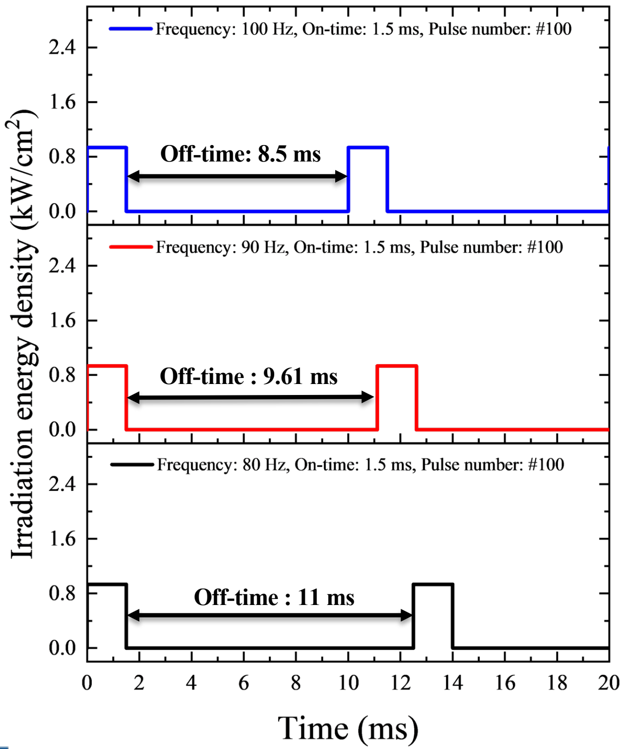
- To verify the effect of pulse on-time, it was irradiated under three conditions (2.25, 1.5, and 1 ms).
- The shorter the on-time, the higher the temperature achieved.

❖ Effect of Frequency on Temperature Profile

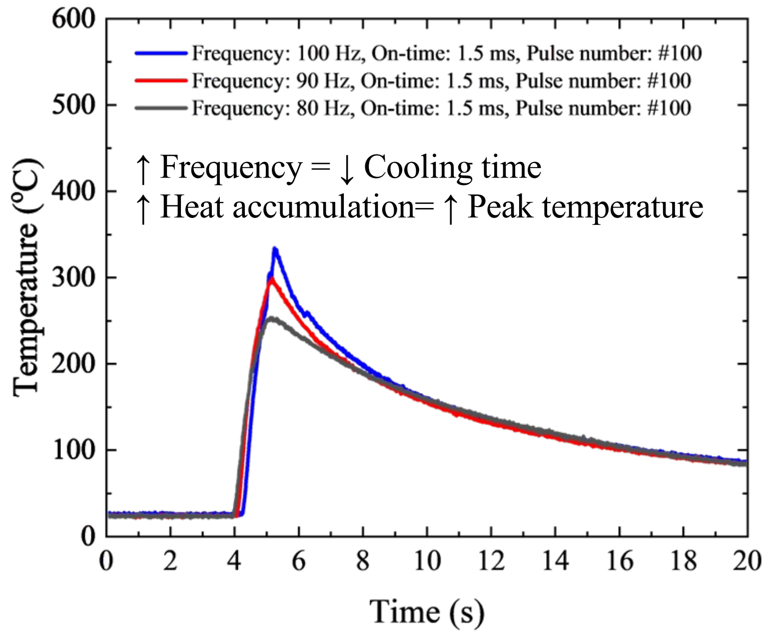
<Back>

▣ IPL parameter with pulse frequency

✓ **Frequency (100 / 90 / 80 Hz)**



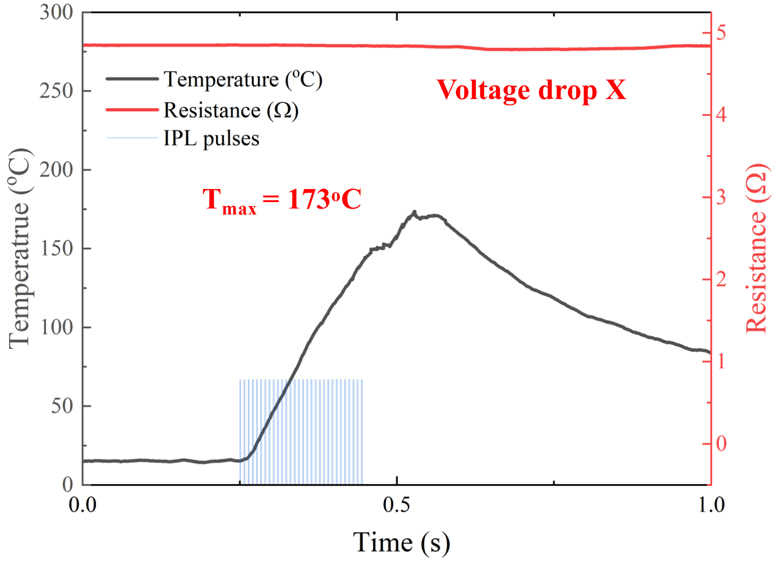
✓ **Temperature profiles during IPL bonding**

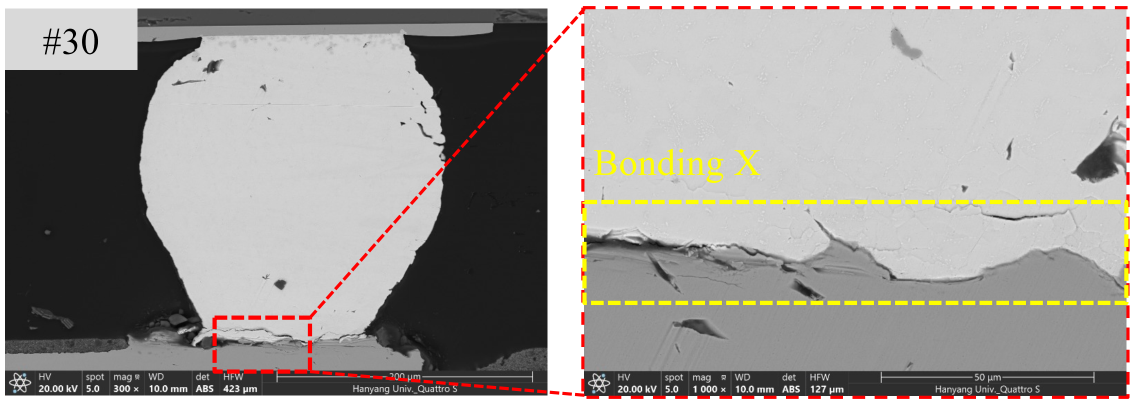


- To verify the effect of frequency, it was irradiated under three conditions (100, 90, and 80 Hz).
- Frequency significantly affects thermal management through cooling time control.

❖ Cross-sectional SEM image of flip-chip package solder joint

Pulse number : #30



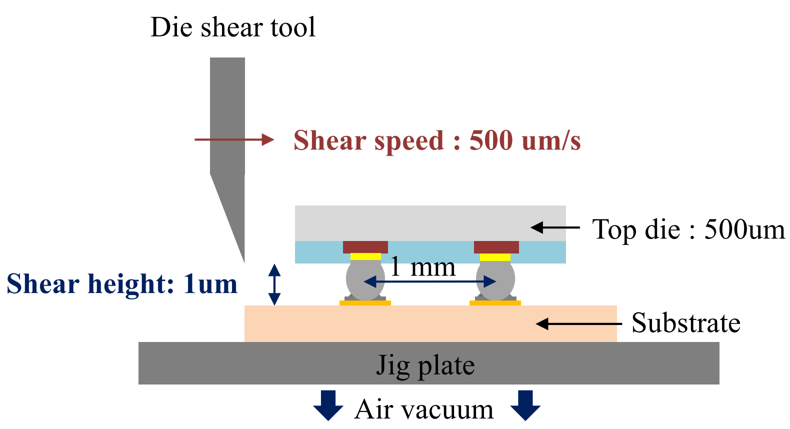


- Temperature monitoring confirmed that 30 pulses generated insufficient thermal energy (173˚C < 217˚C melting point), preventing solder liquidation and bonding.
- Cross-sectional SEM reveals clear bonding failure: no metallurgical interface formation between solder and Cu pad.

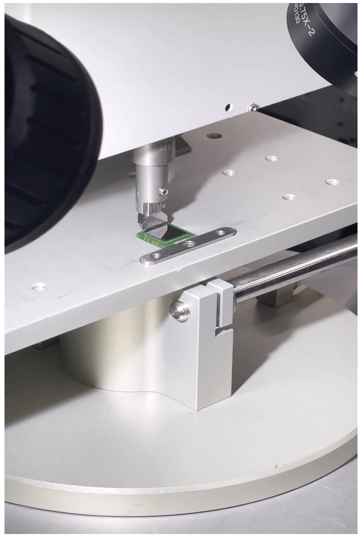
❖ Mechanical Reliability Evaluation by Die Shear Test

<Back>

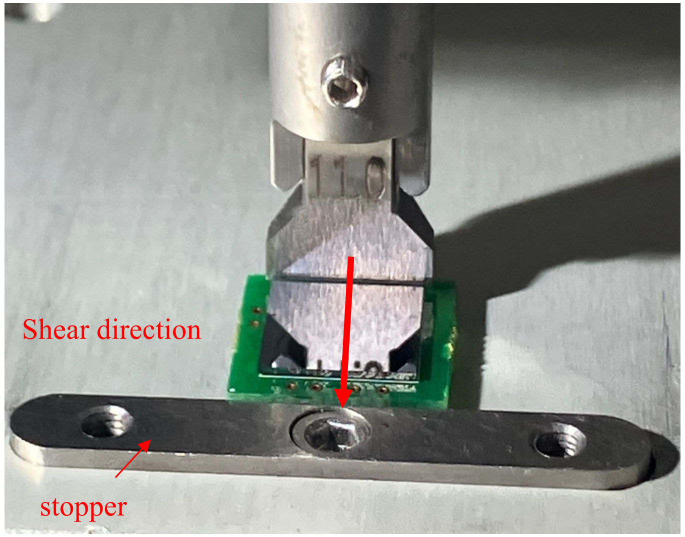
▣ The schematic of die shear test



▲ **Die shear condition**



▲ **Die shear test (Video)**



▲ **Die shear test**

- Die shear testing was performed to quantitatively evaluate the mechanical strength of solder joints produced by optimized IPL process versus conventional reflow.